

CLAIMS

[0067] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A pixel cell comprising:
 - at least one transistor structure comprising:
 - at least one semiconductor channel region;
 - at least one gate for controlling the channel region; and
 - first and second leads respectively coupled to a source region on one side of the at least one channel region and a drain region on an opposite side of the at least one channel region, wherein the at least one transistor structure has at least two threshold voltages associated with the at least one channel region, and wherein an I-V characteristic of the transistor structure is determined at least in part by the threshold voltages.
2. The pixel cell of claim 1, wherein the at least one transistor structure is an active element for operating at least in part in a sub-threshold region.
3. The pixel cell of claim 1, wherein the at least one transistor structure is a source follower transistor structure.

4. The pixel cell of claim 1, wherein the at least one transistor structure comprises first, second, and third channel regions connected in parallel.
5. The pixel cell of claim 4, wherein the first channel region corresponds to a highest first threshold voltage and the second and third channel regions correspond to second and third threshold voltages, respectively.
6. The pixel cell of claim 4, wherein a first channel region corresponds to a highest first threshold voltage and second and third channel regions correspond to a second threshold voltage.
7. The pixel cell of claim 1, wherein the at least one transistor structure comprises one channel region, and wherein the channel region comprises a normal conduction path and at least one parasitic conduction path.
8. The pixel cell of claim 7, wherein the normal conduction path is associated with a highest first threshold voltage and the at least one parasitic conduction path is associated with at least a second lower threshold voltage.
9. The pixel cell of claim 8, wherein the transistor structure comprises first and second parasitic conduction paths,

- and wherein the first and second parasitic conduction paths are associated with a second threshold voltage.
10. The pixel cell of claim 8, wherein the transistor structure comprises first and second parasitic conduction paths, and wherein the first and second parasitic conduction paths are associated with second and third threshold voltages, respectively.
 11. The pixel cell of claim 1, wherein the two or more threshold voltages result at least in part from the at least one transistor structure having any of: two or more gate oxide thicknesses, two or more channel dopant concentrations, and two or more gate work-functions.
 12. The pixel cell of claim 1, wherein the I-V characteristic is such that a sub-threshold region and a linear region provide a same or similar amplification factor for a signal.
 13. The pixel cell of claim 1, further comprising a photo-conversion device.
 14. The pixel cell of claim 13, wherein the photo-conversion device is a pinned photodiode.
 15. A pixel cell comprising:
a photo-conversion device; and
at least one transistor structure comprising:

first, second, and third semiconductor channel regions;
at least one gate for controlling the channel regions; and
first and second leads respectively coupled to source
regions on one side of the channel regions and drain
regions on an opposite side of the channel regions,
wherein the first channel region is associated with a
highest first threshold voltage, and wherein the second
and third channel regions are associated with at least a
second threshold voltage, and wherein an I-V
characteristic of the transistor structure is determined at
least in part by the threshold voltages.

16. The pixel cell of claim 15, wherein the at least one transistor structure is an active element for operating at least in part in a sub-threshold region.
17. The pixel cell of claim 15, wherein the at least one transistor structure is a source follower transistor structure.
18. The pixel cell of claim 15, wherein the second and third channel regions are associated with second and third threshold voltages, respectively.
19. The pixel cell of claim 15, wherein the two or more threshold voltages result at least in part from the at least one transistor structure having any of: two or more gate

oxide thicknesses, two or more channel dopant concentrations, and two or more gate work-functions.

20. A pixel cell comprising:
 - a photo-conversion device; and
 - at least one transistor structure comprising:
 - a channel region;
 - a gate for controlling the channel region; and
 - first and second leads respectively coupled to a source region on one side of the channel region and a drain region on an opposite side of the channel region, wherein the channel region comprises a normal conduction path and at least one parasitic conduction path, and wherein the normal conduction path is associated with a highest first threshold voltage, and wherein the at least one parasitic conduction path is associated with at least a second threshold voltage, and wherein an I-V characteristic of the transistor structure is determined at least in part by the threshold voltages.
21. The pixel cell of claim 20, wherein the at least one transistor structure is an active element for operating at least in part in a sub-threshold region.

22. The pixel cell of claim 20, wherein the at least one transistor structure is a source follower transistor structure.
23. The pixel cell of claim 20, wherein the channel region comprises first and second parasitic conduction paths, and wherein the first and second parasitic conduction paths are associated with second and third threshold voltages, respectively.
24. The pixel cell of claim 20, wherein the first and at least second threshold voltages result at least in part from the at least one transistor structure having any of: at least two gate oxide thicknesses and at least two channel dopant concentrations.
25. An image sensor, comprising:
 - an array of pixel cells, wherein at least one of the pixel cells comprises:
 - a photo-conversion device; and
 - a transistor structure, the transistor structure comprising:
 - at least one semiconductor channel region;
 - at least one gate for controlling the channel region; and
 - first and second leads respectively coupled to a source region on one side of the at least one channel region

and a drain region on an opposite side of the at least one channel region, wherein the transistor structure has at least two threshold voltages associated with the at least one channel region, and wherein an I-V characteristic of the transistor structure is determined at least in part by the threshold voltages.

26. The image sensor of claim 25, wherein the transistor structure is an active element for operating at least in part in a sub-threshold region.
27. The image sensor of claim 25, wherein the transistor structure is a source follower transistor structure.
28. The image sensor of claim 25, wherein the transistor structure comprises first, second, and third channel regions connected in parallel.
29. The image sensor of claim 28, wherein the first channel region corresponds to a highest first threshold voltage and the second and third channel regions correspond to second and third threshold voltages, respectively.
30. The image sensor of claim 28, wherein the first channel region corresponds to a highest first threshold voltage and the second and third channel regions correspond to a second threshold voltage.

31. The image sensor of claim 25, wherein the transistor structure comprises one channel region, and wherein the channel region comprises a normal conduction path and at least one parasitic conduction path.
32. The image sensor of claim 31, wherein the normal conduction path is associated with a highest first threshold voltage and the at least one parasitic conduction path is associated with at least a second threshold voltage.
33. The image sensor of claim 32, wherein the transistor structure comprises first and second parasitic conduction paths, and wherein the first and second parasitic conduction paths are associated with a second threshold voltage.
34. The image sensor of claim 32, wherein the transistor structure comprises first and second parasitic conduction paths, and wherein the first and second parasitic conduction paths are associated with second and third threshold voltages, respectively.
35. The image sensor of claim 25, wherein the two or more threshold voltages result at least in part from the transistor structure having one or more of: two or more

gate oxide thicknesses, two or more channel dopant concentrations, and two or more gate work-functions.

36. The image sensor of claim 25, wherein the I-V characteristic is such that a sub-threshold region and a linear region provide a same or similar amplification factor for a signal.
37. The image sensor of claim 25, further comprising a photo-conversion device.
38. The image sensor of claim 37, wherein the photo-conversion device is a pinned photodiode.
39. A processor system, comprising:
 - (i) a processor; and
 - (ii) an image sensor coupled to the processor, the image sensor comprising:
 - one or more pixel cells, the one or more pixel cells comprising:
 - a photo-conversion device and a transistor structure, the transistor structure comprising:
 - at least one semiconductor channel region;
 - at least one gate for controlling the channel region; and
 - first and second leads respectively coupled to a source region on one side of the at least one channel region and a drain region on an opposite side of the at least one

channel region, wherein the transistor structure has at least two threshold voltages associated with the at least one channel region, and wherein an I-V characteristic of the transistor structure is determined at least in part by the threshold voltages.

40. A method of fabricating a pixel cell, the method comprising:
- forming at least one transistor structure, the act of forming the at least one transistor structure comprising:
 - forming at least one semiconductor channel region;
 - forming at least one gate for controlling the channel region;
 - forming first and second leads respectively coupled to a source region on one side of the at least one channel region and a drain region on an opposite side of the at least one channel region; and
 - setting at least two threshold voltages associated with the at least one channel region, wherein an I-V characteristic of the transistor structure is determined at least in part by the threshold voltages.
41. The method of claim 40, wherein the at least one transistor structure is formed as an active element for operating at least in part in a sub-threshold region.

42. The method of claim 40, wherein the at least one transistor structure is formed as a source follower transistor structure.
43. The method of claim 40, wherein the act of forming the at least one channel region comprises forming first, second, and third channel regions connected in parallel.
44. The method of claim 43, wherein the act of setting the at least two threshold voltages comprises setting a highest first threshold voltage associated with the first channel region and setting second and third threshold voltages associated with the second and third channel regions, respectively.
45. The method of claim 43, wherein the act of setting the at least two threshold voltages comprises setting a highest first threshold voltage associated with the first channel region and setting a second threshold voltage associated with the second and third channel regions.
46. The method of claim 40, wherein the act of forming the at least one channel region comprises forming one channel region having a normal conduction path and at least one parasitic conduction path.
47. The method of claim 46, wherein the act of setting the at least two threshold voltages comprises setting a

highest first threshold voltage associated with the normal conduction path and setting at least a second threshold voltage associated with the at least one parasitic conduction path.

48. The method of claim 47, wherein the act of forming the at least one channel region comprises forming one channel region having first and second parasitic conduction paths, and wherein the act of setting the at least two threshold voltages comprises setting a second threshold voltage associated with the first and second parasitic conduction paths.
49. The method of claim 47, wherein the act of forming the at least one channel region comprises forming one channel region having first and second parasitic conduction paths, and wherein the act of setting the at least two threshold voltages comprises setting second and third threshold voltages associated with the first and second parasitic conduction paths, respectively.
50. The method of claim 40, wherein the act of setting the two or more threshold voltages comprises forming the at least one transistor structure having any of: two or more gate oxide thicknesses, two or more channel

dopant concentrations, and two or more gate work-
functions.

51. The method of claim 40, wherein the act of setting the two or more threshold voltages comprises setting the two or more threshold voltages such that the I-V characteristic is such that a sub-threshold region and a linear region provide a same or similar amplification factor for a signal.
52. The method of claim 40, further comprising forming a photo-conversion device.
53. The method of claim 52, wherein the act of forming the photo-conversion device comprises forming a pinned photodiode.
54. A method of forming a pixel cell, the method comprising:

forming a photo-conversion device;

forming at least one transistor structure, wherein the at least one transistor structure is an active element for operating at least in part in a sub-threshold region, the act of forming the transistor structure comprising:

forming first, second, and third semiconductor channel regions;

forming at least one gate for controlling the channel regions;
forming first and second leads respectively coupled to source regions on one side of the channel regions and drain regions on an opposite side of the channel regions;
and
setting at least two threshold voltages associated with the channel regions, wherein an I-V characteristic of the transistor structure is determined at least in part by the at least two threshold voltages.

55. The method of claim 54, wherein the act of setting the at least two threshold voltages comprises setting a highest first threshold voltage associated with the first channel region and a second threshold voltage associated with the second and third channel regions.

56. The method of claim 54, wherein the act of setting the at least two threshold voltages comprises setting a highest first threshold voltage associated with the first channel region and second and third threshold voltages associated with the second and third channel regions, respectively.

57. A method of forming a pixel cell, the method comprising:

forming a photo-conversion device; and

forming at least one transistor structure, wherein the at least one transistor structure is an active element for operating at least in part in a sub-threshold region, the act of forming the transistor structure comprising:

forming one semiconductor channel region having a normal conduction path and at least one parasitic conduction path;

forming a gate for controlling the channel region;

forming first and second leads respectively coupled to a source region on one side of the channel region and a drain region on an opposite side of the channel region;

setting a highest first threshold voltage associated with the normal conduction path; and

setting at least a second threshold voltage associated with the at least one parasitic conduction path, wherein an I-V characteristic of the transistor structure is determined at least in part by the threshold voltages.

58. The method of claim 57, wherein the act of forming the channel region comprises forming first and second parasitic conduction paths, and wherein the act of setting the at least second threshold voltage comprises

setting a second threshold voltage associated with the first and second conduction paths.

59. The method of claim 57, wherein the act of forming the channel region comprises forming first and second parasitic conduction paths, and wherein the act of setting the at least second threshold voltage comprises setting second and third threshold voltages associated with the first and second conduction paths, respectively.